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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/625,663	07/26/2000	Robert L. Bortolotto	CER1023-00	6299
26541	7590	08/23/2005	EXAMINER	
Cindy S. Kaplan P.O. BOX 2448 SARATOGA, CA 95070			HYUN, SOON D	
			ART UNIT	PAPER NUMBER
			2663	

DATE MAILED: 08/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/625,663

Applicant(s)

BORTOLOTTI ET AL.

Examiner

Soon D. Hyun

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 19 March 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-40 and 42-53 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 22,30,31,37,38,40,42-45,52 and 53 is/are allowed.
- 6) ☒ Claim(s) 1-21,23-29,32-36,39 and 46-51 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date <u>march 19, 2004</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-5, 7, 9, 10, 19-21, 23-25, 29, 32-34, 36, and 46-49, and 51 are rejected under 35 U.S.C. 102(e) as being anticipated by Francis et al (U.S. Patent No. 6,580,720).

Regarding claim 1, Francis et al discloses an apparatus and a method comprising:

a plurality of interface cards (I/O ports in PI racks in FIG. 15A, col. 15, lines 58-60, and col. 40, lines 39-40) for transmitting and receiving data streams between selected I/O ports;

a cross-connect unit (a hub rack 2 in FIG. 15A) for routing the data streams received from a first set of the plurality of I/O ports to a second set of the plurality of I/O ports (col. 15, lines 58-60 and col. 40, lines 41-47), the cross-connect unit routing each data stream based on an associated matrix (a data base including information regarding a plurality of signal paths presently available for each connection to be established generated by a controller, col. 40, lines 54-56), wherein the associated matrix identifies

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the interface cards (receiving I/O ports) that will receive the data stream (each connection could have more than two signal paths, therefore, two receiving I/O ports are listed for receiving the data stream) and an order (an order of latency, i.e., the more than two possible signal paths for each connection is listed by the latency) that the interface cards (receiving I/O ports) will receive the data stream;

a control unit (controller) for controlling the operation of the apparatus (col. 40, lines 54-60);

a back-plane forming connections between the cross-connect unit (hub rack 2) and each of the plurality of interface cards (I/O ports) (col. 19, lines 61-65).

Regarding claim 2, Francis et al further discloses that the associated matrix (the information regarding a plurality of signal paths presently available for each connection to be established) includes a source point (transmitting I/O port) and a destination point (receiving I/O port) for each section (signaling path) of a data circuit (a connection).

Regarding claims 3, 23, 29, and 51, refer to the discussion for claim 1. Francis et al teaches that the associated matrix includes information for all available signal paths for each connection including a next drop point or destination point (a second receiving I/O port for a signal path having second lowest latency for the connection so that the cross-connect unit can route the data stream to the next drop point if the first receiving I/O port (associated with the signal path having the lowest latency) is unavailable due to inoperable (col. 39, lines 1-12).

Regarding claims 4 and 24, refer to the discussion for claims 1 and 3. It is inherent that the cross-connection unit can continually utilize a next drop point (a third

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receiving I/O port), since Francis et al teaches that the associated matrix includes information for all available signal paths for each connection including the next drop point (the third receiving I/O port for a signal path having third lowest latency for the connection) so that the cross-connect unit can route the data stream to the third drop point if the second receiving I/O port is unavailable due to inoperable (col. 39, lines 1-12).

Regarding claims 5 and 25, refer to the discussion for claim 2. It is inherent that the associated matrix includes a previous point (a first receiving I/O port) for each source point (transmitting I/O port) when the second receiving I/O port is connected, since Francis et al teaches that the associated matrix includes information for all available signal paths for each connection including the first I/O port.

Regarding to claim 7, Francis et al further discloses that each of the plurality of I/O port can be connected to all other of the plurality of I/O ports through the cross connect unit (col. 37, lines 43-46) when all I/O ports use same data transfer protocol..

Regarding claim 9, Francis et al disclose the apparatus (MIPPSS) is an add-drop Multiplexer, since Francis et al disclose the apparatus is connected to user equipment or other MIPPSS (hub-to-hub connection) via either electrical or optical cable (col. 15, line 55-col. 16, line 3), the examiner is in the position the apparatus is an add-drop multiplex in the situation when data is transferred between the user terminal and other MIPPSS.

Regarding to claim 10, it is inherent that the I/O ports include telecommunication cards, since the I/O ports are used to transfer data between users (col. 15, lines 55-67).

Regarding to claim 19. Francis et al further discloses that the cross connect unit is passive (the device does not analyze the transferred data (col. 12, lines 45-50).

Regarding claim 20, refer to the discussion for claims 2 and 3.

Regarding claim 21, refer to the discussion for claims 1 and 3. It is inherent that the first and second receiving I/O ports are receiving the data stream when the first I/O port is inoperable when the first receiving I/O port becomes inoperable during receiving the data stream, since the signal path connecting the second I/O port has next lowest latency.

Regarding claims 32, 33, and 34, refer to the discussion for claims 23-25, respectively. Francis et al further teaches that the method is performed using software (a computer program embodied on a computer readable medium, col. 11, lines 44-51), therefore, it is inherent that there exist code segments to perform the method.

Regarding claims 36, 46, and 47, refer to the discussion for claim 3, Francis et al further teaches that the method is performed using software (a computer program embodied on a computer readable medium, col. 11, lines 44-51), therefore, it is inherent that there exist code segments to perform the method.

Regarding claim 48, refer to the discussion for claims 4 and 47.

Regarding claim 49, refer to the discussion for claims 5 and 47.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

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(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 6, 8, 11-18, 26-28, 35, 39, and 50 are rejected under 35 U.S.C. 103(a) as being unpatentable over Francis et al (U.S. Patent No. 6,580,720).

Regarding claims 6, 26, 35, and 50, refer to the discussion claims 5, 25, 34, and 49, Francis et al fail to disclose explicitly using the previous point (the first receiving I/O port) when the first receiving I/O port becomes operational.

However, it would have been obvious to a person having ordinary skill in the art by the time the invention was made to modify the switching fabric of Francis et al by making it uses the previous point (the I/O interface of the first path) when the interface card (I/O port) become operational. A skilled artisan would have been motivated to do so because the first path is the optimum path (lowest latency path) in the system.

Regarding claims 8, 28, and 39, Francis et al fail to disclose explicitly the interfaces (I/O ports) are Ethernet interfaces. However, Francis et al disclose the system can be used for any data transfer protocol (col. 15, lines 37-40). Therefore, it would have been obvious to a person having ordinary skill in the art by the time the invention was made to make the interfaces (I/O ports) as the Ethernet interfaces (Ethernet I/O ports) transfer data stream based on Ethernet when the user system in figure 15A uses Ethernet protocol.

Regarding claims 11-18, and 27, Francis et al fail to disclose explicitly the interfaces (I/O ports) are WDM, TDM, SONET, SDH, PDH, token ring or FDDI interfaces. However, Francis et al disclose the system can be used for any data transfer

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protocol (col. 15, lines 37-40). Therefore, it would have been obvious to a person of ordinary skill in the art by the invention was made to make the interfaces (I/O ports) as WDM, TDM, SONET, SDH, PDH, token ring or FDDI interfaces depending on the need.

Allowable Subject Matter

5. Claims 22, 30, 31, 37, 38, 40, 42-45, 52, and 53 are allowed.
6. The following is a statement of reasons for the indication of allowable subject matter.

The prior art of record fails to teach that the second interface card which was planned to receive the data stream from the first interface card and transmit the data stream to the third interface card in combination with other elements as recited in claims 22, 30, 37, and 52.

The prior art of record fails to teach that the first one of the remaining interface cards was connected to the second one of remaining cards through the disconnected card(s) prior to the disconnecting cards becoming disconnected from the cross-connect in combination with other element as recited in claims 40 and 43.

The prior art of record fails to teach the step of determining the first interface card that is connected to the second interface card and the third interface card is inoperable in combination with other elements as recited in claims 44 and 45.

Response to Arguments

7. Applicant's arguments filed 03/19/2004 have been fully considered but they are not persuasive.

Regarding claim 1, Applicant argues that "Francis et al does not appear to teach of an associated matrix that identifies interfaces cards that will receive a data stream as well as an order that the interface cards will receive the data stream." Examiner disagrees. As discussed for claim rejection above, the cross-connect unit is routing each data stream based on the information generated by the controller regarding a plurality of signal paths presently available for each connection to be established (col. 40, lines 54-56), wherein the information identifies the interface cards (receiving I/O ports) that will receive the data stream (each connection could have more than two signal paths, therefore, two receiving I/O ports are listed for receiving the data stream). The list has an order of latency, i.e., the more than two possible signal paths for each connection is listed by the latency such that that the interface cards (receiving I/O ports) will receive the data stream according to the order. Therefore, the information is the matrix and the order of latency is the order as recited in claim.

Regarding claim 7, Applicant argues that "Francis et al do not teach each interface card is connected to all other interface cards through the a cross-connect." Examiner disagrees. With reference to col. 37, lines 43-46, Francis et al clearly discloses that each of the plurality of I/O port can be connected to all other of the plurality of I/O ports through the cross-connect unit if all I/O ports use same data transfer protocol.

Regarding claim 21, Applicant further argues that Francis et al do not appear a set of receiving devices all receiving a data stream. Examiner disagrees. The second receiving I/O ports will receive the data stream if the first receiving I/O port becomes inoperable during receiving the data stream, since the signal path connecting the second I/O port has next lowest latency. Therefore, the first and second receiving I/O ports are all receiving the data stream.

Regarding claims 23, 29, 32, 36, and 51, Applicant argues that Francis et al do not teach of a plurality of interface cards receiving a data stream. Examiner disagrees. The second receiving I/O ports will receive the data stream if the first receiving I/O port becomes inoperable during receiving the data stream, since the signal path connecting the second I/O port has next lowest latency. Therefore, Francis clearly teaches a plurality of receiving I/O ports receiving the data stream. Applicant further argues that Francis et al do not appear to teach of generating a matrix that includes a destination point and a next destination point. Examiner disagrees. Refer to the discussion for claim 1 for the matrix. The first receiving I/O port and the second receiving I/O port are the destination point and the next destination point, respectively. Therefore, Francis et al clearly teaches the generated matrix that includes a destination point and a next destination point.

Fro the reasons discussed above, Examiner believes that the claim rejection is proper.

Conclusion

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).


A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

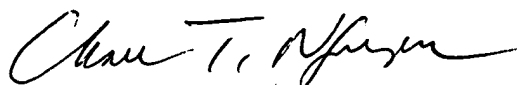
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Soon D. Hyun whose telephone number is 571-272-3121. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ricky Q. Ngo can be reached on 571-272-3139. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).


S. Hyun
08/15/2005



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